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Gold-free growth of GaAs nanowires on silicon: arrays and polytypism

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Abstract
We report growth by molecular beam epitaxy and structural characterization of gallium-nucleated GaAs nanowires on silicon. The influences of growth temperature and V/III ratio are investigated and compared in the case of oxide-covered and oxide-free substrates. We demonstrate a precise positioning process for Ga-nucleated GaAs nanowires using a hole array in a dielectric layer thermally grown on silicon. Crystal quality is analyzed by high resolution transmission electron microscopy. Crystal structure evolves from pure zinc blende to pure wurtzite along a single nanowire, with a transition region.

1. Introduction

III–V nanowires are a key enabler for nanotechnologies and great achievements have been demonstrated in fields ranging from nanoelectronics [1], to nanophotonics [2] and to sensors for biology [3, 4]. The advantages of III–V nanowires include high mobilities, direct bandgaps (except for GaP) and vast possibilities of bandgap engineering. High quality epitaxial nanowires can be obtained on standard, expensive, III–V substrates by either metalorganic vapor phase epitaxy (MOVPE), chemical beam epitaxy (CBE) or molecular beam epitaxy (MBE). However, integration with silicon is desired, since the Si platform is cost-effective and allows for complementary metal oxide semiconductor (CMOS) processing. Nanoscale electronics, photonics and energy applications would greatly benefit from this integration. Yet combining III–V nanowires and silicon represents a difficult technological challenge. Large lattice mismatches between common III–Vs and silicon can lead to misfit dislocations or non-epitaxial nanowires [5, 6]. Control of growth directions is not straightforward, due to the polar nature of binary III–Vs compared to non-polar group IV substrates [7, 8]. Indeed, the preferential nanowire growth direction, ⟨111⟩B, will be vertical at 90° from the surface of a (111)B oriented substrate, whereas four equivalent directions are possible when epitaxially grown on a group IV substrate [9].

Another major challenge arises from the very common use of gold for seed particles to promote nanowire growth in the ⟨111⟩ crystallographic directions, via vapor–liquid–solid (VLS) or vapor–solid–solid (VSS) mechanisms [10]. Although gold performs well for controlled nanowire fabrication, it also diffuses easily on and in silicon, and is well known to create detrimental mid-gap defect states in silicon. This forbids integration of three-dimensional devices based on as-grown gold-seeded III–V nanowires and Si-based processes and electronics. This challenge can be overcome using gold-free nanowire growth procedures, based on either a selective-area growth mechanism [11] or a self-catalyzed growth mechanism [12, 13]. Impressive experimental demonstrations have been made in the area of gold-free III–V nanowire growth, mostly by MOVPE. Controlled growth of arsenides [14–17], phosphides [18], and ternary nanowires [19] in position-controlled arrays has been achieved by this technique. Since the first report of gold-free vertical III–V nanowires grown on silicon [20], recent progress has led to vertical integration

of freestanding nanowire arrays [7, 21], and nanowire devices [22–25].

However, gold-free growth mechanisms have not been studied as much as gold-seeded nanowire growth, and substantial developments are needed both in morphological control and fundamental understanding of the mechanisms. For example, the necessity for oxide on the surface and the need for seed particles remain unclear. Crystal structure is nearly always highly twinned or contains a high density of stacking faults. Very high purity materials are expected by using MBE, thanks to growth in ultra-high vacuum conditions, and to the absence of chemical precursors [26]. However, MBE growth of gold-free III–V nanowires is not yet developed to the level of MOVPE growth. Results focus mostly on GaAs nanowires grown homoepitaxially [27–29], and reports of MBE gold-free nanowires on silicon are scarce [13, 30, 31]. We have reported recently the first antimony-containing axial heterostructure nanowires grown on silicon [32].

In this context, we investigate here growth parameters and structural characterization of self-catalyzed GaAs nanowires directly grown on silicon by MBE. The key influences of growth temperature and V/III ratio are investigated and compared in the case of oxide-covered and oxide-free substrates. We report a precise positioning process for nanowires by defining hole arrays in a thermal oxide on Si(111). Crystal quality is analyzed by transmission electron microscopy (TEM).

2. Experiments

N-doped silicon (111) substrates from Siltronix were selected (resistivity of 3–5 $\times$ 10^{-2} Ω cm). Two protocols were used prior to introduction in the chamber. In the first one, Si substrates were dipped in 5% aqueous hydrofluoric acid (HF) solution for 2 min to remove the native oxide, then rinsed in deionized water for 1 min and blown dry with nitrogen before loading into the introduction chamber, within 20 min. In the second approach, samples were loaded directly into the MBE chamber with no pre-treatment. The surface chemical state, and sample type (by extension), will be referred to in the following as 'oxide-free' and 'oxide-covered' Si. The two types of samples were indium-stuck side by side on an unpolished 2″ Si substrate to allow for comparison and for accurate temperature control during growth.

X-ray photoemission spectroscopy (XPS) experiments were performed with a PHI 5600 model spectrometer to check the complete removal of native oxide after HF treatment. A monochromatic Al Kα source (1486.6 eV) was used, with the analyzer acceptance angle set to 14° and pass energy set to 12 eV. Additional angle resolved XPS measurements (ARXPS) were performed on un-treated silicon substrates to evaluate the thickness of the native oxide layer [33, 34], by varying the polar angle from 37.5° to 70°, relative to the sample surface. Diffraction effects were averaged by rotating the sample with respect to the azimuth.

Temperature was ramped directly to the growth temperature between 570 and 660 °C, always much lower than the temperature required to thermally deoxidize silicon (∼800–900 °C). Growth temperature was measured by both thermocouple and pyrometer. Growth was initiated by opening the arsenic and gallium shutters simultaneously. In some cases indicated in the text, the gallium shutter was opened for a few seconds before GaAs growth, to create mobile gallium droplets on the surface. V/III ratios were calculated from 2D equivalent growth rates of both group III and group V, calibrated by reflection high energy electron diffraction. The GaAs two-dimensional (2D) equivalent growth rate of 1 ML s^{-1} was selected and the V/III ratio was varied by changing group V flux only, in a range from 0.5 to 5. Growth was in most cases terminated by closing the Ga shutter while maintaining the As flux during the cooling down procedure (<2 min). Alternatively, in some cases both group III and V were shut off immediately to facilitate post-growth study of the Ga seed particle. Growth times were typically between 5 and 15 min.

The samples for temperature and V/III ratio series were grown in a solid source MBE (SS-MBE) with uncracked As_4 as the source of group V elements. The GaAs nanowire arrays were obtained in a gas source (GS) MBE using a high temperature cracked AsH_3 gas source (As_2 molecular flow). Recipes have been adapted from one machine to the other quickly, after simple temperature and V/III ratio calibrations. This shows the robustness of the presented results, implemented in the two different standard types of MBE reactors. Results were carefully compared and showed no fundamental differences between the two MBE systems.

Morphology was evaluated by a Zeiss Supra scanning electron microscope (SEM) operated at 10 kV. A JEOL-3000F field emission TEM operated at 300 kV was used for crystal structure characterization in conventional TEM (CTEM) mode and in high-angle annular dark field (HAADF)-scanning TEM (STEM) mode. TEM images were recorded along the $\langle 1\bar{1}0 \rangle$ zone axis (cubic notation) and compositions were determined using x-ray energy dispersive spectroscopy (EDS) operated in HAADF-STEM mode. The presented TEM data were assessed to be representative of all of the NW samples by analyzing 5–10 different NWs for each growth condition.

3. Results

3.1. Influences of the initial chemical state of the surface and growth temperature

In order for the XPS measurements to reflect the real surface chemical state just before nanowire growth is initiated, the loading time after HF treatment ($\leqslant$20 min) and vacuum levels were the same for samples used for surface analysis or growth. The native oxide thickness of the oxide-covered samples has been calculated from ARXPS measurements as recommended by the Consultative Committee for the Quantity of Material [33]. After standard background subtraction according to the Shirley procedure [35], Si 2p core levels were decomposed in five Voigt functions (see insets of figures 1(a) and (b)). A spin orbit splitting of 0.6 eV was used for silicon bulk atoms (Si^0 $2p_{3/2}$ and Si^0 $2p_{1/2}$), and single Voigt functions for silicon atoms bonded to one, three and four oxygen atoms (Si^{1+}, Si^{3+} and Si^{4+} respectively). From these measurements, the native oxide thickness was evaluated to 9 $\pm$ 1 Å. After

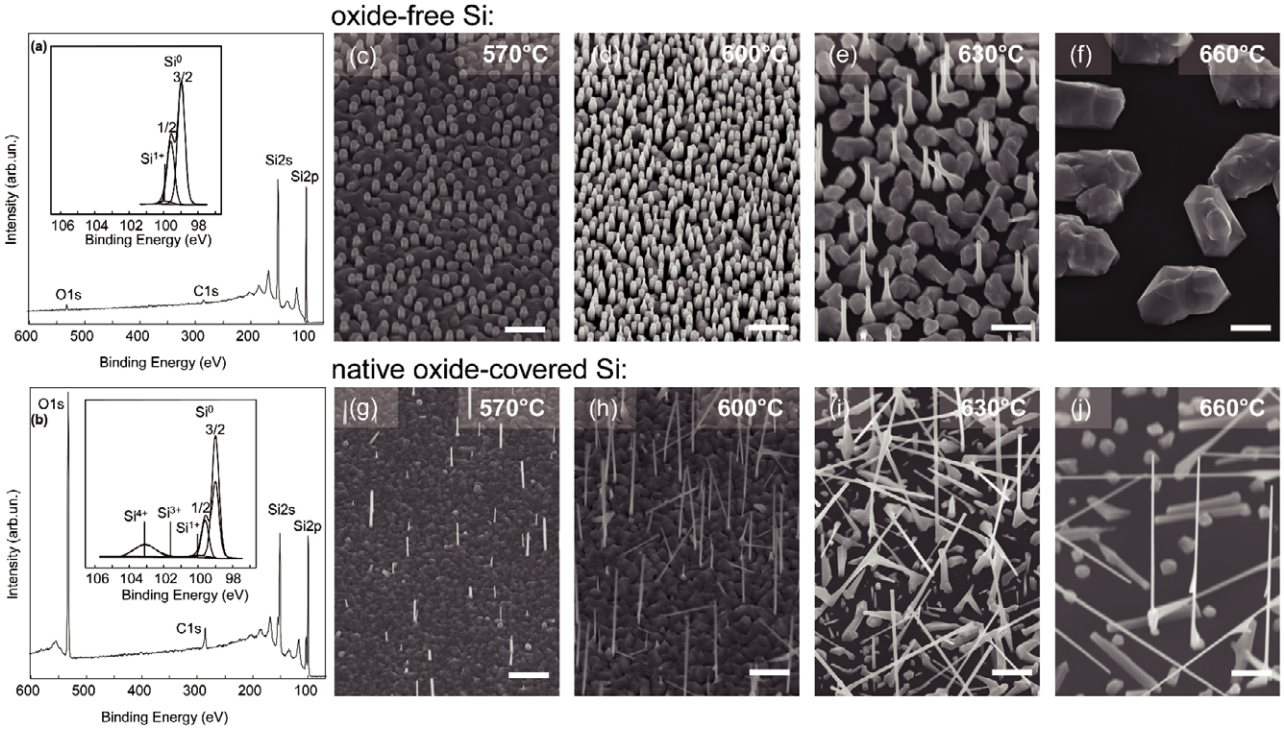

Figure 1. (a) Widescan XPS spectra of the oxide-free and oxide-covered substrates (b) with insets showing high resolution Si 2p core level decompositions. The SEM images (tilt 30°, scale bar 1 μm) show the evolution of nanowire morphology as a function of temperature for oxide-free ((c)–(f)) and native oxide-covered Si ((g)–(i)) substrates. Nanowires shown for each temperature are grown in the same run at each temperature on oxide-free and native oxide-covered silicon.

HF treatment, the O 1s and C 1s peak intensities decrease drastically as shown by the widescan spectra in figures 1(a) and (b). And as confirmed by the high resolution Si 2p spectrum (see inset of figure 1(a)), the HF treatment creates a stable enough passivation to avoid substantial re-oxidation during the time necessary for loading and pumping down to high vacuum. This result is interesting for nanowire growth since the oxide removal is generally performed *in situ* and consists of a time consuming high temperature annealing procedure [23].

The SEM images in figure 1 illustrate GaAs nanowires grown for different temperatures on oxide-free Si(111) (top) and native oxide-covered Si(111) substrates (bottom). If one considers first the oxide-free samples (c)–(f), as temperature is increased from 570 °C (c) to 600 °C (d) and 630 °C (e), striking morphological differences can be seen. At 570 °C, a high density of thick and short nanowires is obtained, then their lengths increase and their diameters decrease with temperature, while observed surface coverage of parasitic bulk growth is continuously reduced. At 660 °C, no nanowires form, and only large crystallites cover the surface. At even higher temperature (720 °C, not shown) nearly no material is present on the surface after the same growth duration. Figures 1(g)–(j) illustrate the temperature evolution of the nanowires grown on native oxide-covered silicon (no HF treatment). As these two different substrate types had been indium-stuck on the same unpolished Si substrate holder and thus grown simultaneously, direct comparison of the growth can be made. At all temperatures, including the highest one (660 °C, figure 1(j)), nanowires are present on oxide-covered Si and their length increases with temperature. Except for the lowest growth temperature (570 °C, figure 1(g)), nanowires are much longer than those grown on oxide-free silicon. No dramatic diameter evolution is observed when increasing temperature (figures 1(g)–(j)), in contrast to nanowires grown under the same conditions on oxide-free substrates (figures 1(c)–(f)). At 570 and 600 °C, parasitic bulk growth is present on the surface, while it is strongly reduced at higher temperatures figures 1(g) and (h). The ratio of straight to kinked and non-epitaxial wires is much lower for all temperatures than for growth on oxide-free samples. Some nanowires grow non-epitaxially, or kink in one of the three non-vertical ⟨111⟩B directions, as seen and explained in previous works [7, 9].

By comparing the growth results on oxide-covered and oxide-free surfaces, one notices that nearly all nanowires grown on oxide-free Si are vertical, over the full range of temperature, while native oxide-covered substrates lead to a high percentage of kinked/non-epitaxial nanowires. However, when grown on oxide-covered substrates, nanowires grow faster and can be grown at higher temperature while minimizing bulk growth between 630 °C (figure 1(i)) and 660 °C (figure 1(j)). Therefore, both oxide-free and oxide-covered Si surfaces seem to offer technologically relevant potentials: vertical yield and high density in the first case, higher vertical growth rate and minimized bulk growth in the second case. The problem of non-epitaxial or kinked nanowires for native oxide-covered Si could originate from its inherent morphology and/or compositional inhomogeneities.

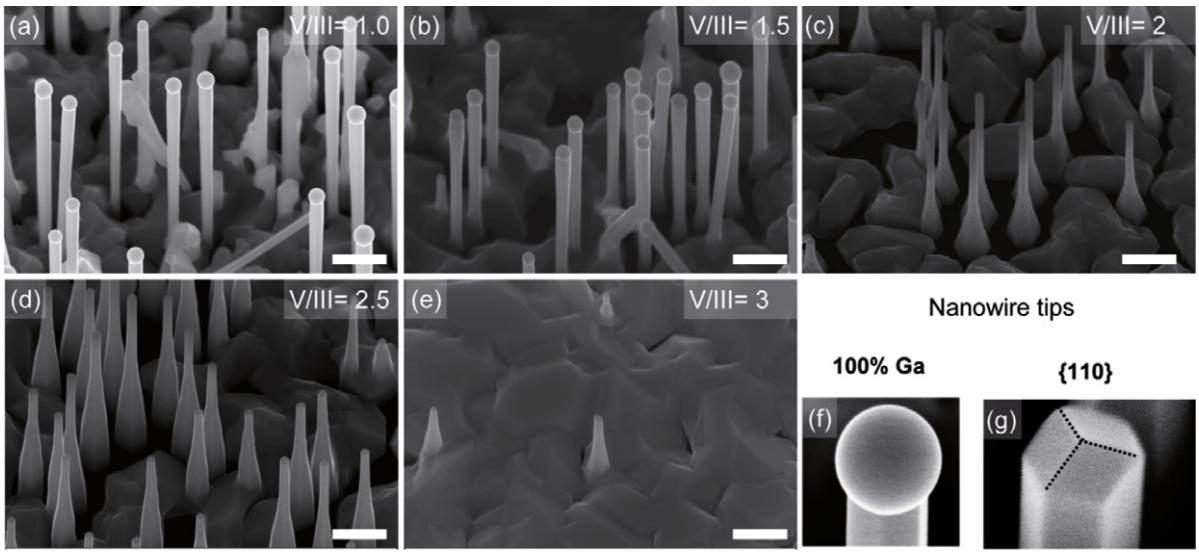

Figure 2. (a)–(e) Evolution of nanowire morphology at 630 °C under increasing V/III ratio for growth on oxide-free Si(111). Growth time is constant for all samples. (f)–(g) Higher magnification of a nanowire tip representative of (a) and (b) and (c)–(e), in (f) and (g) respectively.

Indeed, Fontcuberta *et al* [36] showed that, in the case of SiO_x covered GaAs substrates, very thin silicon oxide could be perforated at random places to allow for epitaxial nucleation of nanowires, while thick enough oxide would lead to non-epitaxial nanowires. On a fundamental level, the nanowire morphology and density evolutions are not easily interpreted. This could be caused by the fact that temperature also influences the effective V/III ratio. Under the conditions studied here, the group III and group V re-evaporation rates are substantial and highly temperature-dependent. A study of the influence of V/III for fixed growth temperature is thus required.

3.2. Influence of V/III ratio

We analyzed the influence of V/III ratio at 630 °C by varying the group V flux while keeping a constant group III flux. A pre-deposition gallium step was introduced for 2 s at 0.25 ML s^{-1} prior to growth, to create mobile gallium droplets on the surface. Growth time is constant for all samples. Only oxide-free samples are shown here for clarity. Similar observations about nanowire shape can be made for oxide-covered Si samples, except that nanowires are longer in that case. SEM images of representative nanowires are shown in figure 2, with increasing V/III ratios from 1 to 3. For a nominal V/III ratio of 1, nanowires have an inverse tapered shape (figure 2(a)), with the top wider than the bottom. By increasing the As flux, the diameter becomes homogeneous over the whole length (figure 2(b)). In figures 2(c) and (d), nanowires are tapered, with a wider base and smaller top diameter. In figure 2(e) the density of nanowires is low and mostly bulk 2D growth is observed. In figures 2(f) and (g) the tops of nanowires grown with low (f) and high (g) arsenic fluxes are shown. Note that growth was terminated in all cases by shutting off Ga, while maintaining arsenic flux during cooling down for 2 min. In figure 2(f), a droplet is visible at the nanowire top. Quantitative energy dispersive x-ray spectroscopy, performed in point analysis mode, proved the particle to be pure Ga. Ga droplet-terminated nanowires were observed for low As fluxes ((a) and (b)). In (g) the nanowire top is terminated by three {110} facets. This was the case for higher As fluxes ((c)–(e)).

From these results, one could suggest that the particle has moved away from the nanowire during cooling down, as in the case of gold-seeded silicon nanowires [37]. Alternatively, as a constituent of the GaAs nanowire, gallium could be incorporated at the nanowire end, in the presence of excess arsenic atoms. From TEM analyses, we will show in the following that this scenario is the relevant one. These observations can be fully explained by a Ga droplet-assisted VLS mechanism [12, 13, 31]. When group V flow is too low, Ga accumulates in the particle over time, leading to a diameter expansion, and as the droplet defines the three-phase boundary at which nanowire growth occurs [38, 39], nanowire diameter increases as well. A slightly higher group V flux leads to a dynamical steady state, where constant Ga droplet size is maintained over the nanowire length. But if group V becomes too high, the Ga droplet shrinks over time and tapering occurs. Some lateral growth via a vapor–solid mechanism (direct incorporation on the sidewalls) cannot be ruled out and could also contribute to the tapering, as a high group V flux reduces group III adatom mobility on the sidewalls. If very high As flux is used (d), the Ga droplet is rapidly consumed and the VLS process is terminated, in favor of 2D bulk growth, as observed here.

The morphological changes observed in figure 2 thus confirm that Ga droplets are the seed particles enabling GaAs nanowire growth and that no nanowire growth can occur when they are absent or consumed. Similar observations are made in the case of native oxide-covered substrates (not shown). This growth mechanism is very different from the one reported for MOVPE-grown arrays on oxide-patterned surfaces [11] where no droplets are ever observed after growth. From our observations of gallium droplets and successful growth on oxide-free silicon, we conclude that oxide is not necessary

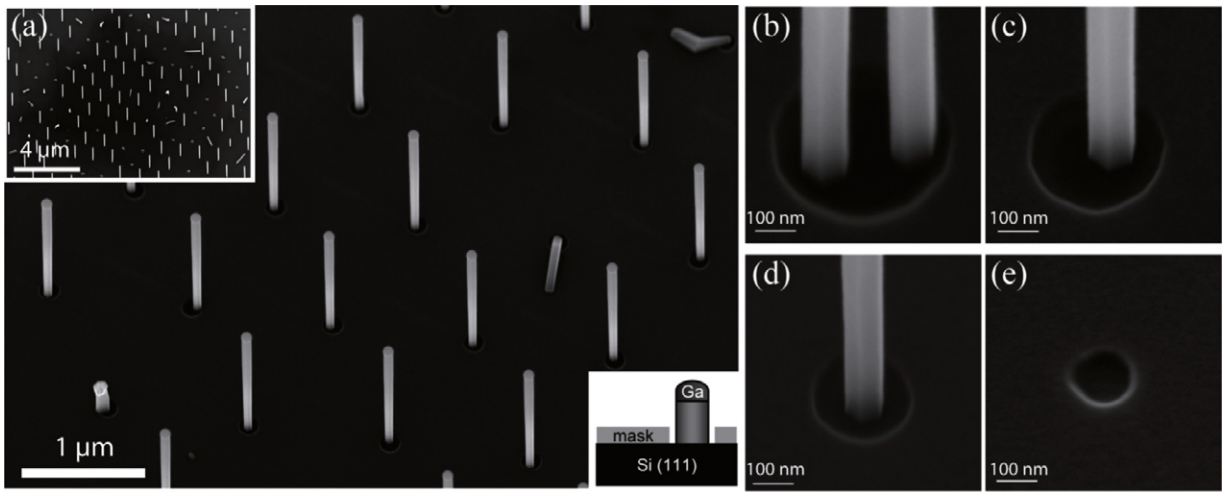

Figure 3. SEM images (tilt 30°) of an array of GaAs nanowires grown using an oxide mask on Si(111). (a) Overview of the array. The insets show a lower magnification image of the array (top left) and a schematic of the nanowire and the oxide mask (bottom right). (b)–(e) Typical higher magnification images of the base of nanowires when grown in holes of different diameters.

to grow Ga-assisted GaAs nanowires. However we will see later that a controlled thermal oxide layer with holes can play an important technological role. Moreover, the fact that the gallium droplet size can be controlled *in situ* opens two interesting possibilities: direct diameter control over length, and natural implementation of core–shell heterostructures, by suppressing the particle under arsenic flux after growth of the core [40].

3.3. Positioning GaAs nanowires on silicon

From the results discussed above, high temperature in combination with a thin oxide layer seems to be the most desirable process-orientated solution, provided that a higher yield of straight epitaxial nanowires can be achieved. Instead of using the thin native oxide as a natural mask, we realized hole arrays in a thermally grown SiO_2 layer using a conventional top-down process. Patterns are defined in a positive resist (PMMA) by electron beam lithography on a 30 nm thick oxide layer, then etched by a standard combination of plasma and chemical etching processes (final oxide thickness of about 20 nm). The template obtained is close to what is used in MOVPE by other groups [7, 41]. To the best of our knowledge, no ordered array of gold-free MBE-grown arsenide or phosphide III–V nanowires has been reported up to now.

Figure 3 illustrates gallium-assisted nanowire growth in such an array. Nanowires are grown at 630 °C using a V/III ratio of 2 in GS-MBE; no gallium pre-deposition step was used in this case. In figure 3(a), a representative illustration of nanowires grown in a hexagonal array of holes is shown. The yield of perpendicular nanowires of identical length is about 60% under the current conditions with base diameter ranging from 45 to 60 nm. In some holes, crystallites or non-epitaxial nanowires are formed. Arrays with different hole diameters were defined on the same substrate, and high magnification SEM images of the resulting nanowire growth are shown in figures 3(b)–(d). When a hole is large (220±5 nm, figure 3(b)), multiple nanowire nucleations can occur. For smaller holes (160 ± 5 nm, figure 3(c), and 120 ± 5 nm, figure 3(d)), only one nanowire per hole is observed. Finally, when holes are too small (70 ± 5 nm, figure 3(e)) no nanowire (or crystallite) nucleation occurs. Note that under optimized SEM imaging conditions, a thin oxide layer could be distinguished in the holes, extending for about 15 nm from the periphery of the mask edges. This means that effective completely oxide-free openings should be smaller than the nominal hole diameter.

As can be seen in figure 3, the relation between holes and nanowire diameters is not straightforward. A wide oxide-free area close to the arrays was designed to serve as a reference. In this area (not shown), all nanowires grow vertically, and have approximately the same diameter as for all nanowires grown in the arrays. This shows that growth conditions (V/III ratio and temperature) primarily determine the nanowire morphology; the nanowire diameters are not directly related to the size of the holes in the array. However, a threshold exists in terms of hole diameters, below which no nanowires nucleate (figure 3(e)) and there is a precise range of hole diameters which allow a single nanowire to nucleate (figures 3(c) and (d)). This demonstrates that the process presented here is relevant for precise positioning of gallium-nucleated nanowires, allowing future vertical device processing. The yield reported here is lower than the perfection reported recently on silicon by MOVPE [7, 21], but this work was based on a mature selective-area nanowire growth mechanism and it was shown that growth conditions/pre-growth procedures were critical to obtain such a yield. We are confident that similar fine tuning will also allow for perfect arrays in the future using our process or a similar process in MBE, and that the process could extend to other group III-nucleated nanowires.

3.4. Crystal structure of GaAs nanowires

Having obtained good control over morphology, yield and position using temperature, V/III ratio and patterned oxide arrays, we now investigate the nanowire crystal structure.

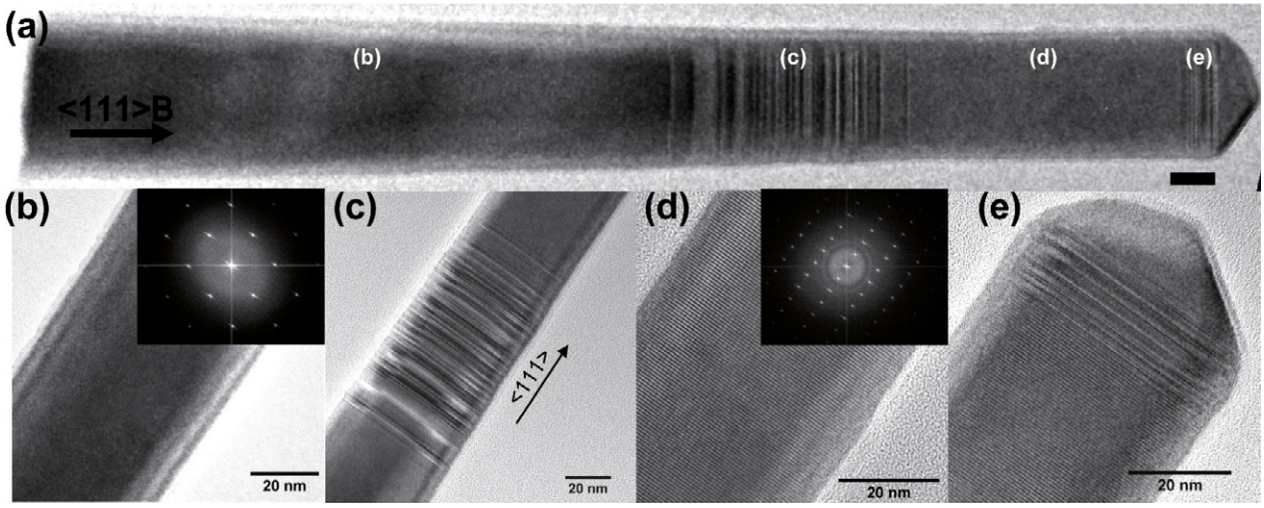

Figure 4. (a) TEM image of a full GaAs nanowire, viewed in the $\langle 1\bar{1}0\rangle$ zone axis (cubic notation). The sample was grown on oxide-free silicon at 630 °C, with V/III = 1.8. The bottom of the nanowire has a ZB crystal structure, with very low stacking faults density in the segment. Then a transition with twin planes and stacking faults occurs in the middle, before a pure WZ structure is observed (right). The neck region forms a ZB tip with a transition region containing stacking faults below. Higher magnification images of the bottom, middle segment, and top including neck are shown respectively in (b), (c), (d). The inset fast Fourier transforms (FFT) show a pattern characteristic of ZB structure (b) and WZ structure (c).

The nanowire shown in 4(a) was grown under our optimized conditions (630 °C, V/III ratio = 2.5) on oxide-free Si, broken off from the substrate, and viewed along the $\langle 1\bar{1}0\rangle$ direction. A contrast due to stacking faults is visible at approximately two thirds of the distance from the bottom (left). Higher magnification images are shown for a selected region of figure 4(a) in (b)–(e), with fast Fourier transform (FFT) of the full image as inset for figures 4(b) and (d) revealing the segment crystal structure. It is observed in all nanowires grown under different V/III ratio that nanowire growth starts as perfectly pure zinc blende with no twin plane or stacking fault (figure 4(b)), then a transition region composed of dense stacking faults occurs, extending over about 100 nm on average (figure 4(c)). The transition region is found to vary from nanowire to nanowire both in exact position within a nanowire and in length (50–150 nm). Some variation in position relative to the base is expected due to the fact that nanowires could break off at different heights from the substrate. However differences in nanowire growth rate for different diameters may also cause variations in both transition region length and position relative to the base and tip.

After this transition region, the upper segment of the nanowire is pure WZ with no stacking faults (figure 4(e)). As this sample was cooled down under arsenic flow, the seed Ga droplet was transformed into the nanowire apex, with a last change of structure from WZ to pure ZB for the apex. The change in crystal structure from ZB to WZ with length was also observed for nanowires grown at a low V/III ratio of 1.5, for which the Ga droplet increased in size during growth. For this sample the transition region was more extended in length, but followed exactly the same sequence of structural changes. A similar transition may also have been seen by others, even if no specific description was given in the text [31]. The fact that the neck region has a different crystal structure than the nanowire below indicates that V/III ratio and/or temperature strongly affects Ga-nucleated GaAs crystal structure. Indeed Spirkoska *et al* found that the V/III ratio affects phase purity in homoepitaxially grown Ga-nucleated nanowires [42].

In order to study the potential influence of the substrate preparation on crystal structure, nanowires grown on oxide-covered Si (in the same growth run) were also investigated by high resolution TEM. A representative example of a nanowire broken off from the native oxide silicon grown samples is shown in figure 5. Although these nanowires are considerably longer than the ones grown on deoxidized substrates, the same trend is observed: after the perfect ZB base (figure 5(b)), a mixed region begins a few hundred nanometers from the bottom of the nanowire (figures 5(c) and (d)). Finally, nearly perfect WZ (single stacking fault density below 1 μm^{-2}) occurs (figure 5(e)). It is noteworthy that no other transition occurs once the nanowire has adopted the WZ phase. The nanowire tip region, corresponding to the Ga droplet crystallization into GaAs under the As flow, is again of ZB phase (figure 5(e)).

Since the transition region is longer for nanowires grown on oxidized substrates, it is possible to investigate more carefully how the nanowire crystal structure evolves from a pure zinc blende crystal to a pure wurtzite crystal. Single twin planes first appear, then dense twin planes, eventually forming stacking faults (two sequential twin planes) [43], then the stacking fault density increases up to the point where WZ dominates. Finally, the density of stacking faults in the WZ phase decreases until nearly perfect WZ is obtained.

It is interesting that the same crystal phase change is observed for nanowires grown on an oxide-free Si and on native oxide-covered Si substrates, since the growth rate is much faster on the latter (see figure 1). This could exclude growth rate as a key parameter controlling this transition, in contrast to effects observed in GaAs gold-nucleated nanowires [44]. The position of the transition region

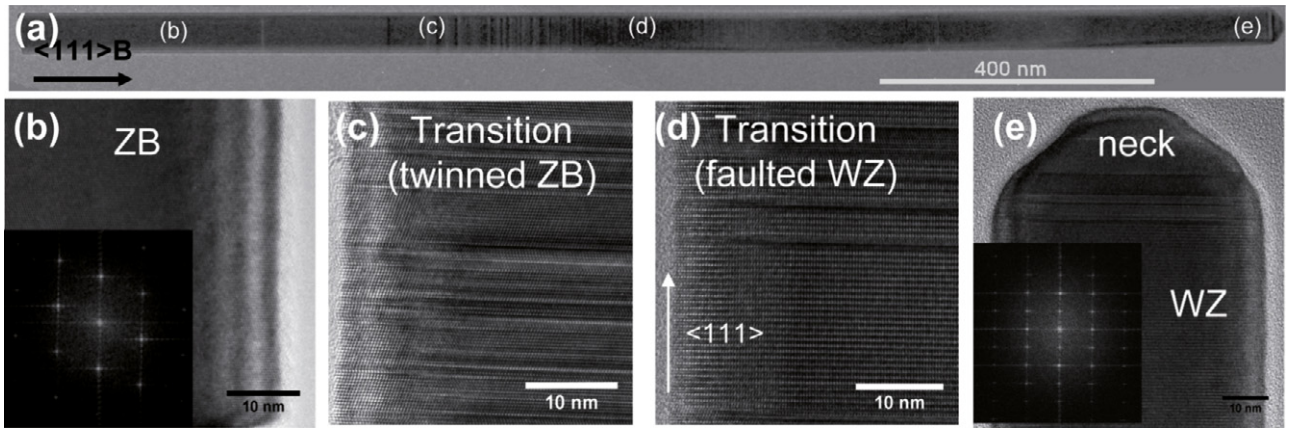

Figure 5. (a) TEM image of a full GaAs nanowire, viewed in the $\langle 1\bar{1}0 \rangle$ zone axis (cubic notation). The sample was grown on oxide-covered silicon at 630 °C, with V/III = 2.5. The bottom of the nanowire has a ZB crystal structure, with very low stacking faults density in the segment. The transition regions show the appearance of a twin plane first then stacking faults up to WZ creation. The top part is pure WZ. The neck region forms a ZB tip with a transition region containing stacking faults below. Higher magnification images of the bottom, middle segment, and top including neck are shown respectively in (b), (c), (d). The inset fast Fourier transforms (FFT) show a pattern characteristic of ZB structure (b) and WZ structure (c).

close to the substrate suggests that the diffusion length along the nanowire sidewalls could play a role in the crystal phase change. Cornet *et al* observed a change of phase purity for gold-nucleated InP nanowire with length [45] and proposed that the group III supersaturation in the gold particle was reduced for long nanowires. However in our case gallium supersaturation should always be close to unity, as gallium is the seed particle allowing for nanowire growth. Therefore the fundamental mechanisms behind this change of crystal structure will require further investigations, outside the scope of the present paper.

4. Conclusion

In conclusion, we have investigated growth parameters for gold-free GaAs nanowires on silicon and shown that the V/III ratio controls the morphology and that temperature controls the amount of parasitic bulk growth. The combination of simple HF treatment and growth under ultra-high vacuum conditions makes it possible to include pre-growth processing of the substrate while avoiding annealing steps before growth. Oxide-free silicon allows for a nearly perfect yield of vertical nanowires but lacks the possibility to control the nanowire position on the substrate. Hole arrays in thermally grown SiO_2 provide a precise way to grow nanowire arrays, with excellent selectivity at high temperature. The grown nanowires have pure crystal phases, with a transition over a short distance from pure zinc blende to pure WZ. Such dramatic complete change of crystal structure opens the way for future design of pure crystal phase arrays of nanowires having either type of crystal structure.

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